

requests may be further qualified based on the scheduling constraints and a command stack of memory request is then developed for modifying update queues. The controller also functions by receiving a controller clock signal and generating an SDRAM clock signal by dividing this controller clock signal.--

IN THE SPECIFICATION:

Page 9, line 31, change "jnidcates" to --indicates--.
Page 10, line 8, change "asume" to --assume--.
Page 15, line 17, change "324" to --322--; and
line 21, change "359" to --354--.

IN THE CLAIMS:

Please cancel claims 12 and 24 without prejudice or disclaimer and amend claims 8, 11 and 23 as follows:

Claim 8, line 6, change "pluarlity" to --plurality--.

Sub B3
11. (Amended) A system for interfacing a processing device with a synchronous DRAM comprising:

means for developing memory requests from the processing device; and

a controller for maximizing throughput of said memory requests from the processing

~~device to the synchronous DRAM based on scheduling constraints of the synchronous DRAM and arbitrating between conflicting memory requests so that data slots used by the synchronous DRAM are maximized.~~

~~AS Sub B~~ 23. (Amended) A method for interfacing a processing device with a synchronous DRAM, comprising the steps of:

- (a) developing memory requests from the processing device; and
- (b) maximizing throughput of said memory requests from the processing device to the synchronous DRAM ~~based on scheduling constraints of the synchronous DRAM and arbitrating between conflicting memory requests so that the data slots used by the synchronous DRAM are maximized.~~

REMARKS

Claims 1-11 and 13-23 are now present in this application.

Applicants greatly appreciate the Examiner's thorough review of the present application and the indication of allowable subject matter in dependent claims 4-8 and 16-20. The present application has been amended to address the